Computer Organization

Academic Year: (2023 / 2024) **Review date: 23-03-2023**

Department assigned to the subject: Systems Engineering and Automation Department

Coordinating teacher: CASTILLO MONTOYA, JOSE CARLOS

Type: Electives ECTS Credits : 6.0

Year : 3 Semester : 2

Branch of knowledge: Engineering and Architecture

REQUIREMENTS (SUBJECTS THAT ARE ASSUMED TO BE KNOWN)

- Programming (1st course, 1st semester)
- Computer Structure (2nd course, 1st semester)
- Operating Systems (2nd course, 2nd semester)
- Computer Architecture (3rd course, 1st semester)

OBJECTIVES

The objective of this course is for the student to learn about the evolution and internal structure of computer architectures and the main factors that influence the performance of a computer. Among the concepts that will be studied in depth are: (i) the necessary conditions for parallelism, (ii) the design of the instruction repertoire, (iii) the microarchitecture of the processor, and (iv) the main internal parallelism techniques that are applied in current processors to improve their performance (caches in the processor, dynamic instruction scheduling, hop prediction, superscalarity). Finally, superscalar, supersegmented and VLIW machines will be discussed as an evolution of processors searching for a higher degree of instruction-level parallelism.

DESCRIPTION OF CONTENTS: PROGRAMME

1. Introduction to computation in parallel. Concept of parallelism and historic evolution.
2. General organization of a computer.
3. Conditions for the parallelism and analysis of the abilities. Analysis of dependencies. Levels of parallelism process and size of the grain. Characteristics of the performance. Theory performance models.
4. Segmentation fundaments. Basic concepts about segmentation. Structures for controlling functional segmented units.
5. Segmented processors. Basic stages of a segmented processor with a static instructions planning. Types of risks and their possible solutions. Multicicle performance. Dynamic instructions planning. Dynamic jumps prediction.
6. Superscalar structures, supersegmented and VLIW. Superscalar and supersegmented processor concept. Uses of a superscalar processor and of supersegmented ones. VLIW processors.

LEARNING ACTIVITIES AND METHODOLOGY

1. Theory classes. Presentation of the main concepts. Discussion and clarification of doubts about the concepts. We will work on transparencies that will be given to students to facilitate learning and a text or basic reference texts required in the course. (2,5 ECTS)
2. Classes of practical exercises. Sessions in which problems are posed, and students are left in groups to present their solutions. (2,5 ECTS)
3. Laboratories. Students (in small teams) will be offered practical case studies, and they should study them and then take the simulation data and analyze it. Knowledge of the topics covered in masterclasses and practical classes in the subject will be used. A preliminary study will be carried out, work will be carried out in the laboratory, and a written report will be delivered with the results and proposed solutions. (1 ECTS)

ASSESSMENT SYSTEM

The course evaluation is based on a continuous model. The student mark will take into consideration the activities in the course. The course has a theoretical and a practical part.

The continuous evaluation of the theoretical and practical parts will be assessed through two partial exams.
* If the student passes both exams and has attended all practical parts (laboratory sessions), the student passes the course. If any of the practical parts are not attended for any reason, the student have to contact his/her professor to recover it.
* If one of the mid-term exams is not passed the student will have a recovery exam for the failed part.
The mark in the course will be the average between the passed exams (if both are passed) or between the passed and recovery exams (if passed).
* If both mid-term exams are not passed, the student will have a recovery exam for the whole course and that score will be the final one.
* A student can go to the recovery exam to improve his/her mark on one mid-term exam (o both), but the score considered will be the one obtained in the recovery exam.

The four practical sessions are required to pass the course.

Parcial exams constitute the total course score.

Addendum COVID 19

Due to the situation with COVID 19, the continuous evaluation will be carried out through personal work that will be worth 20% of the continuous evaluation and a single partial exam (with problems on both parts) that will be carried out online that will be worth 80% of continuous evaluation. The grade of the continuous evaluation will be the sum of both parts and will be considered approved when said sum is greater than or equal to 5.

If the pass is achieved, it will not be necessary to take the final recovery exam, you can go to the final exam if you have not passed the partial exam.

% end-of-term-examination:	0
% of continuous assessment (assigments, laboratory, practicals…):	100

BASIC BIBLIOGRAPHY

- J. L. HENNESSY y D.A. PATTERSON Computer Architecture: A Quantitative Approach, Fourth Edition. Ed Elsevier 2007.
- J. SILC et al, ¿Processor Architecture¿, Springer Verlag, 1999.

ADDITIONAL BIBLIOGRAPHY

- A.R. OMONDI The Microarchitecture of Pipelined and Superscalar Computers, Kluwer Academic Publishers, 1999.
- H. S. STONE High Performance Computer Architecture, Ed Addison Wesley, 1993.
- P. M KOGGE The Architecture of Pipelined Computers, Ed Mc Graw Hill, 1981.