System-on-Chip and efficient electronic circuit integration techniques

Academic Year: (2023 / 2024) **Review date: 28-04-2023**

Department assigned to the subject: Electronic Technology Department

Coordinating teacher: PATON ALVAREZ, SUSANA

Type: Electives ECTS Credits : 3.0

Year : 1 Semester : 2

REQUIREMENTS (SUBJECTS THAT ARE ASSUMED TO BE KNOWN)

- Analog and Digital Subsystem Design (O)
- Techniques and tools for electronic systems design (O)

OBJECTIVES

Learning outcomes acquired by the student:

- Knowledge on the current state-of-the-art on integrated circuits and the different fields of application
- The ability to design analog and mixed-signal circuits for different applications
- Knowledge on the different strategies to optimize power consumption in mixed signal integrated circuits
- Knowledge on specific tools for simulation, design and physical implementation (layout) of ASICs.

DESCRIPTION OF CONTENTS: PROGRAMME

The state-of-the-art for CMOS Application Specific Integrated Circuits (ASIC) and their applications will be described stressing the implications on circuit design and introducing the concept of Systems-on-Chip (SoC), as well as some simulation and design (including layout) tools for ASICs. Different mixed signal front-end circuits for Integrated Circuits (IC) and ASICS will be described and the intended applications. These descriptions will be used to classify circuits in terms of functionality, power consumption, size and figures-of-merit such as linearity, noise immunity and so on, of capital importance for ICs and ASCIs design. Finally, techniques for power consumption reduction and performance enhancement will be presented through several circuit examples.

LEARNING ACTIVITIES AND METHODOLOGY

Learning activities:
-Theoretical classes
-Practical classes: They will be carried out with free circuit simulation software and lay-out tools.
-Theoretical-practical classes
-Tutorials

ASSESSMENT SYSTEM

The evaluation system consists of the following sections:
- A test exam or short questions that is taken at the middle of the course and that assesses basic theoretical knowledge (20%).
- A collection of practical works: design exercises, simulations and lay-out of small blocks and some system (40% in total). The evaluation of this part will be based on the deliveries of the students, and may be complemented with an individual practical knowledge quiz.
- Final exam based on problems and short questions with a weight of 40%, with a minimum requiered mark of 3.5 out of 10

% end-of-term-examination:	40
% of continuous assessment (assigments, laboratory, practicals…):	60

BASIC BIBLIOGRAPHY

- Baker, R. Jacob CMOS: circuit design, layout, and simulation, IEEE Press, 2005
- Sansen, Willy M. C. Analog design essentials, Springer, 2006

ADDITIONAL BIBLIOGRAPHY

- Johns, David Analog integrated circuit design, John Wiley & Sons, 1997