Computer Technology

Academic Year: (2021 / 2022) **Review date: 01-07-2021**

Department assigned to the subject: Department of Electronic Technology

Coordinating teacher: MARTIN GONZALEZ, HONORIO

Type: Basic Core ECTS Credits : 6.0

Year : 1 Semester : 2

Branch of knowledge: Engineering and Architecture

OBJECTIVES

The objective of this course is to introduce students to the operation, analysis, and design of digital circuits. The fundamentals of hardware description languages and digital circuit design in VHDL will also be introduced.
At the end of this course, the following skills will have been acquired:
- Know the purpose and basic operation of digital circuits
- Analyze and use digital circuits
- Design digital circuits

DESCRIPTION OF CONTENTS: PROGRAMME

1. Information representation in digital systems
1.1. Introduction to digital systems
1.2. Number systems. Conversions between number systems
1.3. Binary codes
2. Boolean Algebra and logic functions
2.1. Postulates and fundamental properties of Boolean Algebra
2.2. Boolean functions and expressions
2.3. Logic gates. Characteristics of logic gates.
2.4. Implementation of logic functions with logic gates
3. Introduction to digital circuit design using VHDL
3.1. Introduction to Hardware Description Languages. The VHDL language
3.2. Basic concepts of VHDL design
3.2.1. Entities and architectures
3.2.2. Ports and signals
3.2.3. Concurrent and sequential statements
3.2.4. Basic data types
4. Basic combinational circuits and VHDL description
4.1. Encoders
4.2. Decoders
4.3. Multiplexers
4.4. Demultiplexers
4.5. Combinational circuit description in VHDL
4.5.1. Conditional statements
4.5.2. Rules for the design of combinational circuits in VHDL
4.5.3. Application examples
5. Arithmetic combinational circuits and VHDL description
5.1. Representation of signed numbers
5.2. Binary arithmetics
5.2.1. Addition and substraction
5.2.2. Multiplication and division
5.3. Representation of real numbers
5.4. Arithmetic circuits
5.4.1. Adders and substractors
5.4.2. Multipliers
5.4.3. Arithmetic Logic Units (ALUs)
5.5. Implementation of arithmetic circuits in VHDL
5.5.1. UNSIGNED and SIGNED types
5.5.2. Use of arithmetic operators

6. Flip-flops
6.1. Asynchronous latches
6.2. Synchronous flip-flops
6.3. Timing characteristics
6.4. Synchronous circuits
6.5. Circuits with flip-flops: waveforms
7. Synchronous sequential circuits and VHDL description
7.1. Registers
7.2. Counters
7.3. Design of sequential circuits in VHDL
7.3.1. Flip-flops and registers
7.3.2. Rules for the design of sequential circuits
7.3.3. Counter design
7.4. Finite State Machines (FSMs)
7.4.1. Moore and Mealy models
7.4.2. Analysis of synchronous sequential circuits
7.4.3. Design of FSMs in VHDL
8. Memories and VHDL description
8.1. Types of memories
8.2. Characteristics of memories
8.3. Memory access waveforms
8.4. Extension of memory size
8.5. Implementation of logic functions with memories. FPGAs
8.6. Modeling of memories in VHDL. Application examples
9. Introduction to digital systems and microprocessors
9.1. Structure of a digital system: data path and control
9.2. Characteristic components of a digital system
9.3. Digital system design at the Register Transfer level
9.4. Architecture of a basic microprocessor
9.5. Basic operation of a microprocessor. Instructions

LEARNING ACTIVITIES AND METHODOLOGY

1. Lectures: 1 ECTS. Intended to reach the specific competences of the course. Students will receive class notes and reference books in order to work and get in-depth knowledge on the course contents.
2. Practice:1 ECTS. Design and development of digital circuits with the aid of the professor. Intended to develop the procedural competences and most of the general competences. They will also contribute to develop the attitudinal competences.
3. Student work:3,5 ECTS
- Exercises and complementary lectures proposed by the professor.
- Personal study
4. Exercises and exam: 0,5 ECTS

ASSESSMENT SYSTEM

Assessment: 70% on-going evaluation.

On-going evaluation is decomposed into:
- Midterm exams: Exam 1 (25%) y Exam 2 (30%)
- Lab Practice and exercises: 15%. Assistance to these sessions is compulsory.

Students must attend all laboratory sessions to complete on-going evaluation

Evaluación: 70% evaluación continua.

La nota de evaluación continua se descompone en los siguientes pesos:
- Exámenes parciales: Parcial 1 (25%) y Parcial 2 (30%)
- Prácticas y ejercicios: 15%.

Para completar el proceso de evaluación continua es obligatorio asistir a todas las sesiones prácticas.

Final exam 30%
Second call grade is 100 % of the final exam mark.

% end-of-term-examination:	30
% of continuous assessment (assigments, laboratory, practicals…):	70

BASIC BIBLIOGRAPHY

- FLOYD, T.L. "Fundamentos de Sistemas Digitales (Digital Systems Fundamentals)", Prentice-Hall.
- HAYES, J.P. "Introducción al Diseño Lógico Digital (Introduction to Digital Logic Design)", Addison-Wesley.