Analog and digital subsystems design

Academic Year: (2021 / 2022) **Review date: 26/05/2021 10:59:05**

Department assigned to the subject: Electronic Technology Department

Coordinating teacher: ENTRENA ARRONTES, LUIS ALFONSO

Type: Compulsory ECTS Credits : 6.0

Year : 1 Semester : 1

OBJECTIVES

SKILLS
- Students must have the knowledge and understanding that provide a basis or opportunity for originality in developing and/or applying ideas, often within a research context.
- Students should be able to apply their knowledge and their problem-solving skills in new or unfamiliar environments within broader (or multidisciplinary) contexts related to their field of study.
- Students should be able to integrate knowledge and handle complexity, and formulate judgments based on information that, being incomplete or limited, includes thoughts about the social and ethical responsibilities related to the application of their knowledge and judgments.
- Develop concise, clear and justified documentation, and specify the work to be done for the development, integration and implementation of complex and high added value electronic systems.
- Ability to devise, design, implement and maintain an electronic system in a specific application.
- Acquire skills for understanding new technologies in use in electronic systems, and use and integrate them properly to solve new problems or applications.
- Adopt the scientific method as a fundamental working tool in both professional and research environments.
- Ability to design electronic systems at the behavioral level, from a given set of specifications, at system level, using modeling and simulation tools , and at subsystem level, using hardware description languages.
- Ability to use advanced tools, techniques and methodologies for the design of electronic systems or subsystems.
- Ability to design a device, system or application that meets a given specification, using a systematic and multidisciplinary approach, and integrating modules and advanced tools that are specific to the field of Electronic Engineering .

LEARNING OUTCOMES
The students passing this course should be able to:
- Specify and design advanced analog subsystems for instrumentation, audio, industrial control and communications such as conditioning amplifiers, data conversion, power and switching amplifiers, and switched capacitor circuits.
- Know the latest technologies and architectures of digital systems, and be able to specify and devise digital architectures from system specifications.
- Specify and design complex digital subsystems in an optimal manner, by selecting the most adequate technologies and processing elements, and taking into account the system performance and the use of resources (cost/area, power).
- Know High-Level Synthesis tools and tools for the hardware description o analog, digital and mixed-signal circuits.
- Use advanced signal analysis techniques, such as spectral analysis (DFT, FFT, spectral estimation), conversion techniques of discrete-continuous systems (residues, impulse invariance) applied to digital signal processing, statistical analysis of continuous and sampled signals, quantization error, shot noise and thermal noise.
- Evaluate the impact of noise in electronic systems and use low-noise design techniques.

DESCRIPTION OF CONTENTS: PROGRAMME

1. Fundamentals of Register-Transfer Level (RTL) design
1.1. Digital systems and abstraction levels
1.2. Structure of a digital system at the RT level: data path and control
1.3. General purpose architectures: the microprocessor
1.4. Application-specific architectures. Hardware Acceleration
2. Design Evaluation and Optimization (I)
2.1. Area estimation
2.2. Delay estimation
2.2.1. Delay analysis and modeling
2.2.2. Timing constraints
2.2.3. Static Timing Analysis (STA)
2.3. Design optimization for area and performance at the logic level
2.3.1. Optimization at the logic level
2.3.2. Technology mapping
2.3.3. Optimization strategies
2.4. Design optimization for area and performance at the RT level
2.4.1. Serial implementation
2.4.2. Parallel implementation
2.4.3. Pipelined implementation
2.4.4. Retiming
3. High-Level Synthesis
3.1. Fundamentals of High-Level Synthesis
3.2. Data Flow Graph Analysis
3.3. Scheduling
3.3.1. Time constrained scheduling
3.3.2. Resource constrained scheduling
3.4. Allocation and binding
3.5. System throughput and interfaces
3.6. Application examples
4. Design Evaluation and Optimization (II)
4.1. Power estimation
4.1.1. Power analysis and modeling
4.1.2. Power estimation techniques
4.2. Design optimization for power consumption
4.2.1. Dynamic Voltage & Frequency Scaling (DVFS)
4.2.2. DVFS architectures
4.2.3. RTL and logic power optimization techniques
4.2.4. Clock gating
4.2.5. Dynamic power management
4.3. Clocking issues
4.3.1. Clock generation: PLLs
4.3.2. Clock distribution
4.3.3. Clock domain crossing. Metastability
5. High-level Synthesis with Vivado HLS
5.1. Introduction.
5.2. Project creation, validation and synthesis
5.3. Optimization directives
5.4. Loops
5.4.1. Loop unrolling
5.4.2. Loop pipelining
5.5. Arrays
5.6. Data types and bit accuracy
5.6.1. C/C++ data types
5.6.2. Bit accurate data types
5.6.3. Quantization and overflow modes
5.6.4. Floating point support
5.7. Optimizing resource utilization
5.8. Interfaces
5.8.1. Basic signaling and handshaking
5.8.2. Memory I/O protocols: RAM and FIFO
5.8.3. Bus I/O protocols

5.9. Application examples

Analog Subsystems

1. Introduction
2. Continuous Time Active Filters
2.1. Basic Concepts. Types of electronics filters.
2.2. Synthesis of filters.
2.3. First order filters.
2.4. Second order filters.
2.5. Applications and Examples.
3. Noise in Electronic Circuits
3.1. Introduction.
3.2. Random Time Domain Signals.
3.3. Random Frequency Domain Signals.
3.4. Noise Types.
3.5. Noise Models for circuits components.
3.6. Sampled noise.
4. Sample & Hold Circuits. Analog Multiplexers
4.1. Problem to solve.
4.2. Operating basics
4.3. Basic Implementation
4.4. Load Injection
4.5. Opening Uncertinty
4.6. Practical Circuits and Applications
5. Switched capacitor circuits
5.1. Elements of a switched capacitor circuit
5.2. Basic Integrator
5.3. Discrete Integrator insensitive to parasitic capacitances with delay
5.4. Discrete Integrator insensitive to parasitic capacitances without delay
5.5. Adder and gain stages
5.6. Discrete time Filters of first and second order
6. Principles of A/D and D/A. D/A converters
6.1. Noise a uniform quantizer
6.2. Static parameters of an A/D and D/A, static errors, INL and DNL
6.3. Dynamic parameters. SNR, SNDR, SFDR, ENOB and dynamic range
6.4. D / A converters with resistance networks
6.5. D / A converters with current sources
6.6. D / A converters with switched capacitors
6.7. Converter with R-2R network
6.8. Integrating A/D Converters (ramp, dual ramp)
6.9. Succesive approximation A/D converters (SAR)
6.10. Pipe-line A/D converters
6.11. FLash A/D converters
7. Oversampled Circuits
7.1. Concept of oversampled systems
7.2. Principle of noise shaping (Noise Shaping)
7.3. Sigma-delta modulators of 1st and 2nd order
7.4. Implementation of oversampled A/D
7.5. Implementation of oversampled D/A converters
8. Time encoded circuits
8.1. Types of Frequency Synthesizers
8.2. Dynamic Equations of a phase control loop (PLL)
8.3. Elements of a PLL: phase comparators, LC VCO, programmable dividers
8.4. DDS Synthesizers
8.5. Ring Oscillators. Time to Digital Converters
8.6. Digital PLL Synthesizers

LEARNING ACTIVITIES AND METHODOLOGY

LEARNING ACTIVITIES
Lectures
Theoretical and practical classes
Practical classes

TEACHING METHODOLOGIES
Teacher explanations supported with audiovisual media and information technology, in which the main concepts of the subject are developed and the reference literature is provided to supplement student learning.
Demonstration of practical cases, problems, etc.. The cases are posed by the teacher and solved individually or in groups with support of information technology.

ASSESSMENT SYSTEM

% end-of-term-examination/test:	40
% of continuous assessment (assigments, laboratory, practicals…):	60

Continuous evaluation system based on:
- Practical case assignment (20%)
- Mid-term exam of Digital Subsystems (40%)
- Final exam of Analog Subsystems (40%)

Extraordinary Call:
The evaluation will use the continuous evaluation system with the same weights of the first call or a final exam for 100% of the grade

BASIC BIBLIOGRAPHY

- A. Sedra Microelectronic Circuits, Oxford Publishing, 1991

- D. Gajski Principles of Digital Design, Prentice Hall, 1996

- D. Johns Analog Integrated Circuit Design, J. Willey & Sons, 1997

- M. Fingeroff High-Level Synthesis Blue Book, Xlibris, 2010

- null Vivado Design Suite User Guide. High-Level Synthesis, Xilinx, 2014