Integrated circuit design

Academic Year: (2020 / 2021) **Review date: 08-07-2020**

Department assigned to the subject: Electronic Technology Department

Coordinating teacher: ENTRENA ARRONTES, LUIS ALFONSO

Type: Electives ECTS Credits : 6.0

Year : 4 Semester : 1

REQUIREMENTS (SUBJECTS THAT ARE ASSUMED TO BE KNOWN)

Digital Electronics

OBJECTIVES

By the end of this content area, students will be able to have:

1. coherent knowledge of integrated circuit design including the use of advanced professional design tools;
2. the ability to apply their knowledge and understanding to identify, formulate and solve design problems using an appropriate methodology based on the use of hardware description languages, simulation and synthesis;
3. the ability to apply their knowledge and understanding to analyse engineering products, evaluating and optimizing the use of hardware resources and the performance of integrated circuits;
4. the ability to apply their knowledge and understanding to develop and realise designs that meet specified requirements;
5. an understanding of design alternatives (structural, behavioural, IP-based, etc.), and an ability to use them;
6. the ability to design and conduct appropriate simulations and tests, interpret the data and draw conclusions to debug a design;
7. workshop and laboratory skills.
8. the ability to select and use appropriate equipment, tools and methods;
9. the ability to combine theory and practice to solve integrated circuit design problems at RT level;
10. an understanding of applicable techniques and methods to integrated circuit design at RT level and of their limitations;

DESCRIPTION OF CONTENTS: PROGRAMME

1. Introduction to integrated circuits and microelectronics. Design methodology.
- Implementation of digital circuits. Integrated circuits and FPGAs. Pros and cons.
- The design process of an integrated circuit. Design tools. Design flow.
- Hardware Description Languages (HDLs). Pros and cons.

2. Review and extension of VHDL language concepts
- Structural design and component instantiation
- Packages
- Concurrent and sequential statements. Processes.
- Objects. Considerations about the use of variables and signals.
- Data types and operators.
  + Scalar types
  + Composite types: ARRAY and RECORD
  + Subtypes
  + Operators and conversion functions
  + Attributes
  + Synthesis of data types
- VHDL design of combinational circuits
  + Conditional statements and combinational circuits
  + Rules for the design of synthesizable combinational circuits
- VHDL design of sequential circuits
  + Synchronous and asynchronous sequential circuits
  + Rules for the design of synthesizable sequential circuits
  + Register and flip-flop inference

3. Design validation by simulation

- General structure of a test bench
- Stimuli generation
  + Waveform generation using concurrent statements
  + Waveform generation using sequential statements
  + Application examples
- Output checking. ASSERT statement.
- Use of files for input and output

4. Design organization. Generic design.

- Design organization
- Generic design
  + Generic parameters
  + IP blocks
  + Types of IP blocks. Configuration and use.
  + Application examples
- Iterative statements
  + Sequential iterative statements. Loops
  + Concurrent iterative statements
- Subroutines. Functions and procedures.

5. FPGAs

- Introduction. Types of FPGAs
- Internal structure of a FPGA
- Basic resources
  + Logic cells. Operationg modes
  + Input/Output blocks
  + Routing resources
- Advanced resources
  + Memory blocks
  + Arithmetic blocks (DSPs)
  + Clock management and PLLs
  + Other resources
- Configuration
- Examples of FPGA families and devices
- Applications

6. Synthesis and design optimization

- Digital systems and abstraction levels
- Synthesis steps
- Design objectives. Estimation of area and delay.
- Design optimization techniques at different abstraction levels
- Design optimization at the RT level. Serial, parallel and pipelined implementations.
- Clock frequency adjustment. Clock generation.
- Estimation of power consumption. Low power design.
- Examples with tools

LEARNING ACTIVITIES AND METHODOLOGY

- Lectures: 1 session/week (2 h.)
- Practice: 1 session/week (2 h.). Most sessions in Computer Room to develop practical exercises using design tools
- Lab. Practice: 4 sessions, 3 h. each. Devoted to implement a practical circuit
- Personal assistance, as scheduled by the professor

ASSESSMENT SYSTEM

Continuous evaluation system based on:
- Midterm partial exam: 15%
- Design works proposed by the professor, to be carried out in practice sessions and lab sessions: 50%
- Final exam: 35%

It is mandatory to fulfill the design works proposed by the professor.

% end-of-term-examination:	35
% of continuous assessment (assigments, laboratory, practicals…):	65

BASIC BIBLIOGRAPHY

- B. Mealy, F. Tappero "Free Range VHDL. The no-frills guide to writing powerful code for your digital implementations", open-source (http://www.freerangefactory.org/.

- Ott, Douglas E., Wilderotter, Thomas J. "A designer¿s guide to VHDL synthesis", Kluwer Academic Publishers, 1994

- Peter J. Ashenden The Designer's Guide to VHDL, Morgan Kaufmann, 2008

- Peter J. Ashenden Digital Design (VHDL): An Embedded Systems Approach, Elsevier, 2007

- SMITH, D.J. HDL chip design, Doone, 1997

BASIC ELECTRONIC RESOURCES

- Luis Entrena Arrontes, Celia López Ongil, Mario García Valderas, Enrique San Millán Heredia, Marta Portela García, Almudena Lindoso Muñoz . (OCW) Integrated Circuits and Microelectronics: http://ocw.uc3m.es/tecnologia-electronica/integrated-circuits-and-microelectronics